REMARKS

Claims 1-57 and 59 are pending in the application. Claim 58 is canceled by this amendment without prejudice. No claims are presently allowed.

Claim 1 is amended to add a period to the end of the claim.

Claim 21 is amended to clarify that there are first and second tasks, to correct "another processing element" to "the first processing element," and to clarify that the critical section end signal is received from the first processing element.

Claims 26-28 and 32 are amended to correct "sending" to "receiving" as the step recited in the base claim.

Claims 37 and 58 are amended to provide antecedent basis for the execution of instructions.

Claim 52 is amended to correct a spelling error.

Claim 59 is amended to add antecedent bases for "said ring of processing elements."

None of the amendments are narrowing amendments.

It is assumed that paragraph 1 of the office action of 11/09/2004 is an error, as the filing date of the application is wrong, there has not been a restriction requirement, and there were no newly added claims.

Docket Number

Applicants request that the docket number of the application be changed to NC 84,885 in the USPTO records.

Claim Rejections – 35 U.S.C. § 112

Claims 26-28, 32, 37-52, and 58 have been rejected under 35 U.S.C. § 112, second paragraph as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

As for claims 26-28 and 32, the claims were rejected for lack of antecedent basis for "said sending." This has been amended to "said receiving," which is a step recited in the base claim 21.

As for claims 37 and 58, the claims were rejected for lack of antecedent basis for "prior

to executing the critical section instruction" and "suspending execution of the critical section instruction" when the claims do not recite the execution of the critical section instruction. The claims have been amended to recite that the critical section instruction is among a series of instructions to be executed ... at a first processing element. This provides the antecedent basis and makes clear which processing element is executing the instructions. This amendment also overcomes the rejection of claim 38-45, dependent on claim 37.

Claim 46 has been rejected as allegedly unclear as to why the critical section end signal should be received from the second processing element and as to whether two critical sections are the same or different. As to the first point, the purpose of the signal from the second processing element is to trigger the resumption of processing the task at the first processing element. As to the second point, the claim recites only one critical section. The "critical section of the task" is a section, but the "critical section end signal" is a signal and not a task. Dependent claims 47-52 were rejected only for their dependency on claim 46 and are also asserted to comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections – 35 U.S.C. § 103

Claims 1-25, 29-31, and 33-59 have rejected under 35 U.S.C § 103(a) as allegedly unpatentable over Iwasaki et al. (UP 5,274,809).

Claim 1 is to an apparatus for processing information including a plurality of tasks, at least one of the plurality of tasks having a critical section. The apparatus comprises a first processing element coupled to a second processing element. The first processing element includes a critical section end detector and a critical section end signal generator. The second processing element includes a critical section detector and a critical section processing controller. The critical section processing controller is responsive to a critical section end signal received from the first processing element.

Iwasaki discloses system and method of locking and releasing shared resources in a multiprocessor.

In order to make a *prima facie* case of obviousness, each claim limitation must be disclosed in the references. The reference does not disclose the limitation in claim 1 that the second processing element receives the critical section end signal from the first processing element. A critical section is not executed on the second processor until at least one critical

section end signal is received from the first processor, indicating the completion of another critical section on the first processor. The end signal is sent directly from one processor to another. It is not required that the second processor check a table or queue to determine whether execution of its critical section is permitted.

Iwasaki does not disclose critical section end signals sent between processors. Instead, a task that is waiting to use a locked resource must repeatedly consult a resource wait queue to determine whether the resource is available, allowing the task to proceed. The need for the use of the resource may be considered a form of critical section. The critical section is executed no sooner than when the resource becomes unlocked and may also require the waiting task to be dispatched to a processor. It should be noted that Iwasaki does not address the problem of multiple task processing the same data in the correct order. It is possible for a resource to be unlocked and used by a second task while a first task is in an interrupted state. Thus the resource might not contain valid data.

In the present invention, no resource wait queue is needed. An upstream processor directly signals a downstream processor that it may execute a critical section. If the critical section involves processing shared data, the critical section executed at the second processing element cannot be executed and use the shared data until the critical section executed at the first processing element ends.

As all the claim limitations of claim 1 are not disclosed in the reference, a *prima facie* case of obviousness has not been made. Also, no motivation or suggestion to modify the reference and a basis for a reasonable expectation of success are stated, as is required to make a *prima facie* case. There is also no finding of the level of ordinary skill in the art.

Claims 12 and 59 contain all the limitations of claim 1 and asserted to distinguish from the reference in the same manner as claim 1. Claims 2-11 and 13-20 depend from and contain all the limitations of claims 1 and 12, respectively, and are asserted to distinguish from the reference in the same manner as claim 1.

Further, as to claims 2-3 and 18-19, these claims recite a counter that is incremented or decremented in response to a critical section end detector. The Examiner stated that this is equivalent to the counter that indicates the number of lock failures in Iwasaki (col. 10, lines 41-45). However, the counter is Iwasaki is not changed in response to an end detector, which, as stated in the independent claims, is sent from a processing element. The present counter counts

how many critical sections have ended in the upstream processor. The counter in Iwasaki counts failed lock attempts. As the counters count different things, the limitation is not disclosed in the reference.

As to claim 9, this claim recites an instruction that accesses a shared variable. The Examiner stated that the shared variable is disclosed in the abstract of Iwasaki. However, the abstract does not mention variables or data, and shared variables are not mentioned anywhere. As stated above, Applicants contend that Iwasaki would not preserve the integrity of shared variables.

As to claims 12 (13-20 dependent thereon) and 59, these claims recite a ring of processing elements. A ring of processing elements is not disclosed in the only cited reference, and so a *prima facie* case of obviousness has not been made. The Examiner stated that a ring is not precluded by Iwasaki, but this is not sufficient to disclose it.

The Examiner also stated that it would have been obvious to use the resources in series and reduce overhead due to the simplicity of the arrangement. However, a ring of processing elements is not the same as a series. A series implies a beginning and ending, where the last element is not directly connected to the first. A ring has no inherent beginning or ending without a designation from outside the ring to begin the processing, such as from a host control processor. This is not as simple as a series. Further, is it not explained how a series reduces overhead.

Claim 21 is to a method for processing tasks on multiple processing elements. A first task is processed on a first processing element. Processing of a second task on a second processing element is inhibited based on processing a critical section instruction at the second processing element. A critical section end signal is received at the second processing element from the first processing element. The critical section end signal indicates completion of processing of a critical section of a task at the first processing element. Processing of the second task at the second processing element is resumed based on the critical section end signal.

As explained above, the reference does not disclose that the first processing element sends the critical section end signal directly to the second processing element, and so a *prima facie* case has not been made. Claims 22-36 depend from and contain all the limitations of claim 21, and are asserted to distinguish from the reference in the same manner as claim 21.

As to claim 35, this claim recites an instruction that accesses a shared variable. The

Examiner stated that the shared variable is the lockword of Iwasaki. However, the lockword is a means for locking a resource. It does not represent data that is to be operated on by both processing elements, as is a shared variable.

Claim 37 is to a method for controlling access to shared resources while processing network data elements on multiple processing elements. A critical section instruction is detected among a series of instructions to be executed while processing a network data element at a first processing element. Prior to executing the critical section instruction, an end critical section signal counter associated with a second processing element is checked. If the end critical section signal counter is not above a threshold value, execution of the critical section instruction is suspended.

The Examiner stated that it is well known to use a counter and an upper limit to prevent monopolization of a resource by one task. However, the counter in claim 37 does not count the amount of time that a processing element is using a resource. It counts the number of critical sections that have been executed on a processing element. Counting the critical sections may be necessary to ensure program synchronization (paragraph 0076). Without the counter, a critical section may perform operations on data that is not valid.

Claims 38-45 depend from and contain all the limitations of claim 37, and are asserted to distinguish from the reference in the same manner as claim 37. Further as to claim 44, the argument from claim 35 above applies.

Claim 46 is to a method for performing parallel processing. Processing of a task at a first processing element is suspended in response to detecting a beginning of a critical section of the task. Processing of the task at the first processing element is resumed in response to a critical section end signal received from a second processing element.

As explained above, Iwasaki does not disclose sending a critical section end signal from one processing element to another, and so a *prima facie* case has not been made. Claims 47-52 depend from and contain all the limitations of claim 46, and are asserted to distinguish from the reference in the same manner as claim 46.

As to claims 47 and 52, as explained above, Iwasaki does not disclose a ring of processing elements.

As to claim 51, as explained above, Iwasaki does not disclose a critical section end counter.

Claim 53 is to an apparatus for processing multiple data elements wherein processing operations include a plurality of tasks, one or more of which having a critical section. The apparatus comprises a ring of processing elements, a first processing element in said ring of processing elements, and a second processing element in said ring of processing elements. The first processing element includes a critical section operative state element and a critical section end signal generator. The second processing element is coupled to the first processing element and includes a critical section detector.

As explained above, Iwasaki does not disclose a ring of processing elements, and so a *prima facie* case has not been made. Claims 54-57 depend from and contain all the limitations of claim 53, and are asserted to distinguish from the reference in the same manner as claim 53. Further as to claim 56, the argument from claim 35 above applies.

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

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